Serial No. 10/666,024
Atty. Dckt. No. 10030557-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.   :   10/666,024   Confirmation No. : 7952
Appellant   :   Reid Hayhow
Filed   :   9/18/2003
TC/A.U.   :   2117
Examiner   :   Phung M. Chung

Docket No.   :   10030557-1

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

Dear Sir:

 This Reply Brief is submitted in response to the Examiner's Answer mailed July 15, 2009.

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Argument

Claims 1-16 should not be rejected under 35 USC 103(a) as being unpatentable over Hughes, Jr. (US Pat. No. 4,493,079; hereinafter referred to as "Hughes") in view of Regelman et al. (US Pat. No. 6,574,626; hereinafter referred to as "Regelman").

Claims 1, 7-10, 14 & 15:

In rejecting claim 1, the Examiner's Answer states at the bottom of page 3 that,

> . . .The called pattern and the dependencies are then selectively copied from the secondary memory to the primary memory prior to executing the called pattern (see col. 2, lines 21-24, lines 31-34, lines 60-67 to col. 3, lines 1-5) is to determine a required memory needed to execute a plurality of test vectors or making sure there is a significant amount of memory needed to execute a plurality of test vectors.. . .

The above sentence seems to be missing some words before or after the parenthetical cites, and appellant cannot discern what point the Examiner is trying to make. However, none of the above Regelman cites teach or suggest "determining a required memory needed to execute [a] plurality of test vectors".

Further, with respect to claim 1, the Examiner asserts that Regelman discloses a memory management process that determines if there is sufficient room in a primary memory to copy a called test pattern and any additional algorithmic subroutines into the primary memory. The Examiner cites to col. 15, line 50 - col. 16, line 10, and to col. 19, line 47 - col. 20, line 27, of Regelman's disclosure. In these sections, Regelman states, in part:

> . . .If there is no primary valid address value in the loadOffsetInt 504, and the called element type is either the test pattern or algorithmic subroutine type, then space for the called element is allocated in the primary memory 20 using a pattern range variable or a subroutine range variable and a vector count 506 for the called element.. . .The pattern range and subroutine range variables 316,318 are

checked to assure that a total allocated space does not exceed the 4 k that is available.

Col. 15, line 57 - col. 16, line 10.

Claim 1 recites "determining a required memory needed to execute [a] plurality of test vectors". Regelman does not disclose this. Although Regelman discloses a check to determine whether an allocated space exceeds the size of an *available* memory, Regelman does not disclose with specificity how such a check would be performed, and Regelman does not indicate that such a check involves a determination of the "required memory needed to execute [a] plurality of test vectors". Specifically, Regelman does not disclose how a vector count 506 and range variables are used to allocate space in the primary memory 20. For example, how are test patterns stored in the primary memory? Is the vector account 506 equal to the allocated space? These questions are not answered by Regelman. Regelman indicates that, after a called element has been loaded in the primary memory 20, the loadOffsetInt 504 indicates the address of the first instruction in the called element. See, col. 15, lines 51-53. Given that the loadOffsetInt address can change, suggesting that multiple items can be stored in the primary memory 20, what do Regelman's range variables signify? Do they signify the actual size of a called element? Or do they indicate an ending address, such that an invalid address signifies that a called element, in combination with whatever else is stored in the primary memory 20, would exceed the size of the memory? Again, Regelman does not answer these questions, and appellant believes it is speculative, at best, as to whether Regelman actually needs to "determin[e] a required memory needed to execute [a] plurality of test vectors" as part of the check to determine whether allocated space exceeds the 4 k memory that is available.

Claim 1 is believed to be allowable for at least the above reason.

Claims 7-9 should be allowed, at least, because they depend from claim 1.

Claim 10 should be allowed, at least, for reasons similar to why claim 1 should be allowed.

Claims 14 & 15 should be allowed, at least, because they depend from claim 10.

Claims 5 & 6:

Claim 5 recites a very specific method for "determining a required memory needed to execute a plurality of test vectors". The method involves 1) determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file, and then 2) setting the required memory equal to the first memory requirement. Thereafter, and for each additional pin of a tester, 1) a second memory requirement needed for the additional pin to execute the test vectors for the first test is determined, and 2) if the second memory requirement is greater than the first memory requirement, the required memory is set to the second memory requirement.

If appellant understands the rejection of claim 5, the Examiner asserts that 1) Hughes discloses loading vectors into each of a number of pin memories, 2) Regelman discloses a vector counter 506, and 3) it would have been obvious to employ a per pin vector counter in Hughes, such that a memory requirement may be determined for each of a plurality of pins. However, even assuming this to be the case, it is noted that claim 5 does not recite a method for simply determining the different per pin memory requirements for executing a plurality of test vectors. Instead, claim 5 recites a method for using these different memory requirements to estimate a per pin memory requirement for the tester as a whole. That is, the end-product of claim 5 is a single per pin memory requirement, which per pin memory requirement is equal to the largest memory requirement of any pin of the tester.

Claim 5 should be allowed because it depends from claim 1, and for the above additional reason.

Claim 6 should be allowed because it depends, ultimately, from claims 1 and 5.

<u>Claim 16:</u>

With respect to claim 16, the Examiner's Answer continues to admit that neither Hughes nor Regelman disclose using a "required memory" to bill a customer. However, the Examiner's Answer seems to suggest that, because memories can contain certain test modes that are used by a manufacturer to test the memories (BIST?), it would have been obvious to bill customers for the memory required to execute test vectors. Presumably, the Examiner is asserting that a customer is getting billed for the incremental cost of adding BIST functionality to a memory. If this is the Examiner's position, appellant asserts that this is an unreasonable and unsupported interpretation of claim 16. Furthermore, the Examiner has not provided any data to suggest that the cost of memory (which is always decreasing) is in any way based on the incremental cost of adding BIST functionality to the memory.

Conclusion

In summary, the art of record does not teach nor suggest the subject matter of Appellant's claims 1-16. These claims are therefore believed to be allowable.

Respectfully submitted,
HOLLAND & HART, LLP

By: ___/Gregory W. Osterloth/_____
        Gregory W. Osterloth
        Reg. No. 36,232
        Tel: (303) 295-8205